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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Akihiko EBINA et al.

Group Art Unit: 2814

Application No.: 10/052,549 ✓

Examiner: M. D. Pizarro Crespo

Filed: January 23, 2002

Docket No.: 111779

For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE INCLUDING
NONVOLATILE SEMICONDUCTOR MEMORY DEVICES

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

1. This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection, Notice of Allowance, or other action that closes prosecution (e.g., Quayle Action), but before payment of the Issue Fee. Attached is our Check No. 144844 in the amount of \$180.00 in payment of the fee under 37 CFR §1.17(p). Please credit or debit Deposit Account No. 15-0461 as needed to ensure consideration of the disclosed information. Two duplicate copies of this paper are attached.

a. I hereby certify that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(1).

2. An English-language Abstract of the non-English language reference is attached hereto.

08/05/2003 AWDHDAF1 00000172 10052549

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3. A computer-generated English translation of the following Japanese Patent Publication has been obtained from the website of the Japanese Patent Office (<http://www.jpo.go.jp>), and is attached, but has not been reviewed for accuracy. See Reference 4.

Respectfully submitted,



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Date: August 4, 2003

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Form PTO-1449 (REV. 8-83)	US Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 111779	APPLICATION NO. 10/052,549
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		APPLICANT(S) Akihiko EBINA et al.	
		FILING DATE January 23, 2002	GROUP 2814

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
	1	5,408,115	04/1995	CHANG	257	324
	2	5,891,775	04/1999	HISAMUNE	438	267
	3	2000/0053345 A1	03/2003	MORIYA et al.	365	200

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS
	4	JP-A-5-326976 (w/ English Abstract and Translation)	10/1993	JAPAN		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

	5	"Twin MONOS cell with Dual Control Gates", Yutaka Hayashi, Seiki Ogura, Tomoya Saito, Tomoko Ogura, 2000 Symposium on VLSI Technology Digest of Technical Papers.				

EXAMINER	DATE CONSIDERED
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Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.